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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,467	06/30/2003	Ishwardutt Parulkar	SUN-P8374	1597

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EXAMINER	
MEHRMANESH, ELMIRA	

ART UNIT	PAPER NUMBER
2113	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/611,467	PARULKAR ET AL.	
	Examiner	Art Unit	
	Elmira Mehrmanesh	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The application of Parulkar et al., for an "On-chip testing of embedded memories using Address Space Identifier bus in SPARC architectures" filed June 30, 2003, has been examined.

Claims 1-19 are presented for examination.

Information disclosed and listed on PTO 1449 has been considered.

Claims 1, 4-6, 12-15, 16-19 are rejected under 35 USC § 102.

Claims 2, 3, 7-11 are rejected under 35 USC § 103.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4-6, 12-15, and 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Irrinki et al. (U.S. Patent No. 6,067,262).

As per claim 1, Irrinki discloses an integrated circuit (Fig. 2) comprising:

A plurality of memory arrays (Fig. 2, element 100 and col. 6, lines 54-59)

Address Space Identifier (ASI) bus interface logic connected by an ASI bus to the plurality of memory arrays, wherein the ASI bus interface logic controls (Figure 2 shows control, address and data signals connected to the memory) access to the plurality of

memory arrays. Figure 1 shows the memory array (100) is connected to multiplexers (110, 112, 114) via the bus. The bus writes address and data to memory array with WRITE_EN and SYS_ADDRESS (col. 5, lines 51-60 and col. 6, lines 11-27).

A memory control unit connected to the ASI bus interface logic (col. 4, lines 66-67 through col. 5, lines 1-3). Figure 1 shows the state machine/controller (102) is connected via the bus to data (106) and address generators (104), multiplexers (110, 112, 114) to memory array (100).

A memory built-in self-test (MBIST) engine connected (Fig. 2, element 125) to the ASI bus interface logic (col. 5, lines 51-60 and col. 6, lines 11-27) wherein the MBIST engine utilizes the ASI bus interface logic to perform memory testing on at least one of the plurality of memory arrays. Figure 2 shows control, address and data signals connected to the memory) access to the plurality of memory arrays. Figure 1 shows the memory array (100) is connected to multiplexers (110, 112, 114) via the bus. The bus writes address and data to memory array with WRITE_EN and SYS_ADDRESS (col. 5, lines 51-60 and col. 6, lines 11-27).

As per claim 4, Irrinki discloses the MBIST engine generates a test output as a product of the memory testing (col. 5, lines 61-64 and col. 6, lines 29-38 and 46-48).

As per claim 5, Irrinki discloses the MBIST engine institutes an action as a product of the memory testing (col. 5, lines 61-64).

As per claim 6, Irrinki discloses the MBIST engine institutes an action as a product of the memory testing (col. 5, lines 61-64).

As per claim 12, Irrinki discloses a method of memory built-in self-test (MBIST) (Fig. 2, element 125) for an integrated circuit (Fig. 2) having:

A plurality of memory arrays (Fig. 2, element 100 and col. 6, lines 54-59)

Address Space Identifier (ASI) bus interface logic connected by an ASI bus to the plurality of memory arrays (Figure 2 shows control, address and data signals connected to the memory) access to the plurality of memory arrays. Figure 1 shows the memory array (100) is connected to multiplexers (110, 112, 114) via the bus. The bus writes address and data to memory array with WRITE_EN and SYS_ADDRESS (col. 5, lines 51-60 and col. 6, lines 11-27).

A memory control unit connected to the ASI bus interface logic (col. 4, lines 66-67 through col. 5, lines 1-3). Figure 1 shows the state machine/controller (102) is connected via the bus to data (106) and address generators (104), multiplexers (110, 112, 114) to memory array (100).

An MBIST engine (Fig. 2, element 125) connected to the ASI bus interface logic (col. 5, lines 51-60 and col. 6, lines 11-27) the method comprising: utilizing the ASI bus interface logic to perform memory testing on at least one of the plurality of memory arrays. Figure 2 shows control, address and data signals connected to the memory) access to the plurality of memory arrays. Figure 1 shows the memory array (100) is connected to multiplexers (110, 112, 114) via the bus. The bus writes address and data

to memory array with WRITE_EN and SYS_ADDRESS (col. 5, lines 51-60 and col. 6, lines 11-27).

As per claim 13, Irrinki discloses generating a test output as a product of the memory testing (col. 5, lines 61-64 and col. 6, lines 29-38 and 46-48).

As per claim 14, Irrinki discloses instituting an action as a product of the memory testing (col. 5, lines 61-64 and col. 6, lines 29-38 and 46-48).

As per claim 15, Irrinki discloses instituting an action as a product of the memory testing (col. 5, lines 61-64 and col. 6, lines 29-38 and 46-48).

As per claim 16, Irrinki discloses an apparatus for memory built-in self-test (MBIST) (Fig. 2, element 125) for an integrated circuit (Fig. 2) having:

A plurality of memory arrays (Fig. 2, element 100 and col. 6, lines 54-59)

Address Space Identifier (ASI) bus interface logic connected by an ASI bus to the plurality of memory arrays (Figure 2 shows control, address and data signals connected to the memory) access to the plurality of memory arrays. Figure 1 shows the memory array (100) is connected to multiplexers (110, 112, 114) via the bus. The bus writes address and data to memory array with WRITE_EN and SYS_ADDRESS (col. 5, lines 51-60 and col. 6, lines 11-27).

A memory control unit connected to the ASI bus interface logic (col. 4, lines 66-67 through col. 5, lines 1-3). Figure 1 shows the state machine/controller (102) is connected via the bus to data (106) and address generators (104), multiplexers (110, 112, 114) to memory array (100).

An MBIST engine (Fig. 2, element 125) connected to the ASI bus interface logic (col. 5, lines 51-60 and col. 6, lines 11-27) the method comprising: utilizing the ASI bus interface logic to perform memory testing on at least one of the plurality of memory arrays. Figure 2 shows control, address and data signals connected to the memory) access to the plurality of memory arrays. Figure 1 shows the memory array (100) is connected to multiplexers (110, 112, 114) via the bus. The bus writes address and data to memory array with WRITE_EN and SYS_ADDRESS (col. 5, lines 51-60 and col. 6, lines 11-27).

As per claim 17, Irrinki discloses means for generating a test output as a product of the memory testing (col. 5, lines 61-64 and col. 6, lines 29-38 and 46-48).

As per claim 18, Irrinki discloses means for instituting an action as a product of the memory testing (col. 5, lines 61-64 and col. 6, lines 29-38 and 46-48).

As per claim 19, Irrinki discloses means for instituting an action as a product of the memory testing (col. 5, lines 61-64 and col. 6, lines 29-38 and 46-48).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 2, 3, and 7-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Irrinki et al. (U.S. Patent No. 6,067,262) in view of Dreibelbis et al. (U.S. Patent No. 5,173,906).

As per claim 2, Irrinki fails to explicitly disclose the programmability feature.

Dreibelbis et al. teaches:

The MBIST engine (col. 3, lines 14-18) further comprises:

A programmable state machine controller (Fig. 1, element 120)

A programmable data generator connected to the controller, wherein the data generator provides data appropriate for a particular test situation (Fig. 1, element 80)

A programmable address generator connected to the controller, wherein the address generator provides addresses appropriate for the particular test situation (Fig. 1, elements 30, 70)

A programmable comparator connected to the controller, wherein the comparator provides test results information for the particular test situation to the controller (Fig. 1, element 90).

It would have been obvious to one of ordinary skill in the art at the time the invention to use the programmability feature of the Built in test system (BIST) of Dreibelbis et al. in the Built in test system (BIST) of Irrinki et al. for more efficient testing of Integrated Circuit memory.

One of ordinary skill in the art at the time the invention would have been motivated to make the combination because Irrinki et al. discloses his BIST system includes test pattern generation algorithms can be implemented in several different ways (col. 5, lines 15-25). Irrinki et al.'s BIST system consists of the same elements as the Dreibelbis et al. 's BIST system. For instance, Fig. 1 of Irrinki et al.'s shows a state machine controller (102), data generator (106), address generator (104) and a comparator (108). Dreibelbis et al. discloses a programmable BIST system (col. 3, lines 14-18) for testing memories (col. 6, lines 43-48).

As per claim 3, Irrinki discloses the MBIST engine further comprises a storage connected to the controller, wherein the storage contains information for the controller (Fig. 1, element 120).

As per claim 7, Irrinki discloses a memory built-in self-test (MBIST) engine (Fig. 2, element 125) for an integrated circuit (Fig. 2) having:

A plurality of memory arrays (Fig. 2, element 100 and col. 6, lines 54-59)

Address Space Identifier (ASI) bus interface logic connected by an ASI bus to the plurality of memory arrays (Figure 2 shows control, address and data signals connected to the memory) access to the plurality of memory arrays. Figure 1 shows the memory array (100) is connected to multiplexers (110, 112, 114) via the bus. The bus writes address and data to memory array with WRITE_EN and SYS_ADDRESS (col. 5, lines 51-60 and col. 6, lines 11-27).

A memory control unit connected to the ASI bus interface logic (col. 4, lines 66-67 through col. 5, lines 1-3) wherein the MBIST engine utilizes the ASI bus interface logic to perform memory testing on at least one of the plurality of memory arrays. Figure 2 shows control, address and data signals connected to the memory) access to the plurality of memory arrays. Figure 1 shows the memory array (100) is connected to multiplexers (110, 112, 114) via the bus. The bus writes address and data to memory array with WRITE_EN and SYS_ADDRESS (col. 5, lines 51-60 and col. 6, lines 11-27).

Irrinki et al. fails to explicitly disclose the programmability feature.

Dreibelbis et al. teaches:

The MBIST engine (col. 3, lines 14-18) comprising:

A programmable state machine controller (Fig. 1, element 120)

A programmable data generator connected to the controller, wherein the data generator provides data appropriate for a particular test situation (Fig. 1, element 80)

A programmable address generator connected to the controller, wherein the address generator provides addresses appropriate for the particular test situation (Fig. 1, elements 30, 70)

A programmable comparator connected to the controller, wherein the comparator provides test results information for the particular test situation to the controller (Fig. 1, element 90).

As per claim 8, Irrinki discloses a storage connected to the controller, wherein the storage contains information for the controller (Fig. 1, element 120).

As per claim 9, Irrinki discloses the MBIST engine generates a test output as a product of the memory testing (col. 5, lines 61-64 and col. 6, lines 29-38 and 46-48).

As per claim 10, Irrinki discloses the MBIST engine institutes an action as a product of the memory testing (col. 5, lines 61-64 and col. 6, lines 29-38 and 46-48).

As per claim 11, Irrinki discloses the MBIST engine institutes an action as a product of the memory testing (col. 5, lines 61-64 and col. 6, lines 29-38 and 46-48).

Related Prior Art

The following prior art is considered to be pertinent to applicant's invention, but nor relied upon for claim analysis conducted above.

Jamal (U.S. Patent No. 5,568,437), "Built-in self test for integrated circuits having read/write memory".

Kablanian et al. (U.S. Patent No. 5,764,878), "Built-in self repair system for embedded memories".

Irrinki et al. (U.S. Patent No. 5,822,228), "Method for using built in self test to characterize input-to-output delay time of embedded cores and other integrated circuits".

Somasundaram et al. (U.S. Patent No. 5,491,793), "Debug support in a processor chip".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elmira Mehrmanesh whose telephone number is (571) 272-5531. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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